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Comprehensive Phase-Change Memory Compact Model For Circuit Simulation

Corentin Pigot, Marc Bocquet, Fabien Gilibert, Marina Reyboz, Olga Cueto, Vincenzo Della Marca, Paola Zuliani, and Jean-Michel Portal

Abstract—In this paper, a new continuous multilevel compact model for phase-change memory (PCM) is proposed. It is based on modified rate equations with the introduction of a variable related to GST melting. The model is evaluated using a large set of dynamic measurements and shows a good accuracy with a single model card. All fitting parameters are discussed and their impacts are detailed. Full circuit simulation is performed. Good convergence and fast simulation time suggest that this new compact model can be exploited for PCM circuit design.

Index Terms—Compact modeling; Integrated circuit modeling; Phase-change memory; PCM; PCRAM;

I. INTRODUCTION

PHASE-CHANGE memory (PCM) is a non-volatile resistive memory device relying on the phase transition of a small volume in a chalcogenide layer (typically GST). It can be switched from an amorphous high resistive phase to a crystalline low resistive phase by applying a short voltage pulse [1], [2]. This technology is overcoming all of its potential roadblocks and now exhibits rapid switching, extended endurance, high temperature data retention, low power consumption, and good thermal stability under solder reflow conditions [3]–[5].

Device compact models are mandatory to simulate the circuit performance during the back-end design flow step. Consequently, they need to be accurate while ensuring a fast convergence time and a minimal memory usage. Macromodels [6]–[8] and piecewise linear models including a decision module or negative differential resistance [9]–[12] present discontinuities, which are likely to generate convergence issues. Compact models based on rate equations [13]–[17], can be fast and robust. However, despite the enhanced accuracy of some of them, a good correlation with experimental data for any random pulse applied has never been published. Such validations are especially important in a multilevel context, where intermediate resistance level states are exploited. This paper presents a new continuous compact model of phase-change memory, based on comprehensive rate equations. The proposed model is extensively validated by experimental results, in a wide range

of time and temperatures. Using a single model card, the simulation of any random shaped pulse can be achieved, for the very first time. The modeling approach relies on simplified temperature computation, compensated by detailed considerations of the nanophysics inside a PCM cell during programming. The model is efficiently implemented in a Verilog-A code without any decision module to ensure convergence and short simulation time.

Section I describes the model equations and the measurements performed to validate it. Section II presents the correlation between simulations and silicon measurements through a brief extraction flow. Section III is focused on model card parameters with emphasis on their influences and physical meanings. A summary of obtained performances is given in Section IV.

II. MODEL PRESENTATION

A. Model architecture

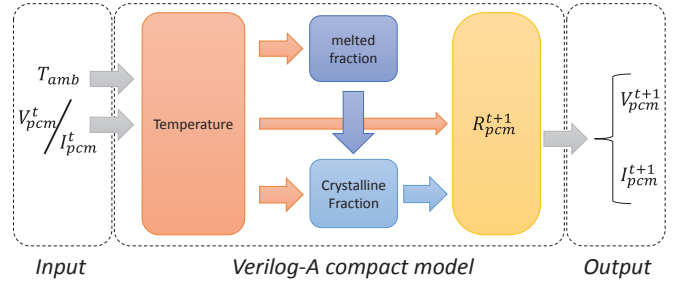


Fig. 1. Modeling flow block diagram

A block diagram of the modeling process is shown in Fig. 1. First, the temperature is computed based on inputs and PCM state from the previous simulation step. The temperature computation module feeds two other related modules: one processing the portion of the active melted volume and the other one determining the crystalline fraction of the remaining non-melted active part. The crystalline fraction and the temperature are then re-input to the DC module, which computes the cell resistance for the current simulation step.

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1) Temperature Module:

Self-heating temperature inside the PCM cell T_{SH} , follows the first order differential equation (1) [13], [18]:

$$R_{th} \cdot C_{th} \frac{\partial T_{SH}}{\partial t} + T_{SH} = R_{th} \cdot \frac{U^2}{R_{PCM}} \quad (1)$$

Where U and R_{PCM} are respectively the voltage across and resistance of the cell, R_{th} and C_{th} are effective thermal resistance and capacitance respectively, and t is the time. The ambient temperature T_{amb} is then added to the self-heating temperature T_{SH} to obtain the final temperature T used in the next calculations. This temperature has no spatial dimension and we consider that it is calculated on a single point in the system, which is the hottest spot of the device. Thermal calculations performed using Cueto *et al.*'s electro thermal solver [19] shown in Fig. 2 indicate that this hottest spot inside the PCM layer is located at the interface between the heater and the amorphous dome.

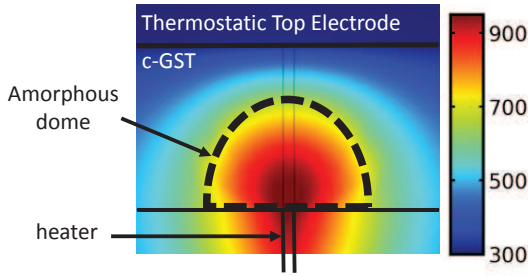


Fig. 2. Finite element simulations of the temperature inside the cell. A temperature gradient is induced between the heater and the top electrode. The simplified temperature calculated in the model refers to the hottest spot.

The effective thermal resistance depends on the phase of the material [15], and has been implemented in the model via the equation (2):

$$R_{th} = R_{thc} \cdot (F_c + F_m) + R_{tha} \cdot F_a \quad (2)$$

R_{thc} is the crystalline thermal resistance and R_{tha} the amorphous thermal resistance. F_c , F_m and F_a are respectively the crystalline, melted, and amorphous fraction of the material.

2) Melting Module

Despite its simplified calculation, the temperature is not considered uniform inside the active volume. Hence, some portion of the material can be melted whereas other parts stay solid during a pulse. This partial melting is implemented by the introduction of the state variable F_m , computed as the solution of the first order differential equation (3):

$$\tau_m \frac{\partial F_m}{\partial t} + F_m = \left[1 + \exp\left(\frac{T_m - T}{\sigma_m}\right) \right]^{-1} \quad (3)$$

Where τ_m is the melting time constant, T_m is the melting temperature of the GST, and σ_m is a parameter reflecting the spatial non-uniformity of the temperature inside the cell. The form of the right hand side of (3) and the fitting parameter σ_m ensure a smooth and continuous transition from solid to melted.

3) Crystalline/Amorphous Module

The crystalline fraction F_c is calculated by modifying the

right hand side of the classical Johnson-Mehl-Avrami-Kolmogorov (JMAK) equation [20] to take the F_m variable into account:

$$\tau_c \frac{\partial F_c}{\partial t} + F_c = 1 - F_m \quad (4)$$

Where τ_c is the characteristic time of crystallization and “1” stands for the whole active area.

The amorphous fraction is then calculated by:

$$F_a = 1 - F_m - F_c \quad (5)$$

When the time becomes infinite, the variable F_c tends to the solid fraction, which is $1 - F_m$, then F_a tends to 0. Indeed, the amorphous phase is seen as a metastable phase, crystallizing even at room temperature. However, this dynamics do not impact the simulation because the crystallization time is long enough.

4) Resistance Module

The resistance of the whole cell is calculated as a series of resistances for each phase, weighted by using their respective fraction:

$$R_{PCM} = F_c \cdot R_c + F_m \cdot R_c + F_a \cdot R_a + R_{heater} \quad (6)$$

Where R_{heater} is the resistance of the heater, which is constant for a given technology. R_c is the resistance of the crystalline phase, and R_a is the resistance of the amorphous phase. We assume that the resistance of the melted phase is R_c because in this state, the current is mainly controlled by the resistance of the poly-crystalline GST surrounding the active area.

The current I_{PF} in the amorphous phase is modeled by Poole-Frenkel conduction [21]–[23] as given by equation (7):

$$I_{PF} = A_{kPF} \cdot F \cdot \exp\left(-\frac{\Phi_{PF} - \beta_{PF}\sqrt{F}}{kT}\right) \quad (7)$$

where A_{kPF} , Φ_{PF} and β_{PF} are fitting parameters with physical meanings described previously [23], and k is the Boltzmann constant. R_a is calculated using the Ohm's law, assuming that the voltage drop inside the PCM is mainly located inside the amorphous dome.

The calculation of the field F , as given by equation (8), is impacted by the thickness of the amorphous cap u_a . u_a is defined in (8) as a fraction of the maximum size $u_{a,max}$ of the dome, the latter being treated as a fitting parameter.

$$F = \frac{U}{u_a} \quad \text{with} \quad u_a = F_a u_{a,max} \quad (8)$$

The Φ_{PF} parameter of (7) follows Varshni's empirical law [24], [25], such that,

$$\Phi_{PF} = E_{a0} - \frac{a_{va} T^2}{b_{va} + T} \quad (9)$$

Where E_{a0} is the activation energy at 0K, considered as a fitting parameter, and a_{va} and b_{va} are thermal parameters, set to the values found in Le Gallo *et al.* [25]: $a_{va}=600\mu\text{eV.K}^{-1}$, $b_{va}=800\text{K}$. The temperature dependence of the resistance during the semi-conducting crystalline phase R_c , follows the expression [26]:

$$R_c = R_{c0} e^{-E_{ac} \left(\frac{1}{kT_{amb}} - \frac{1}{kT} \right)} \quad (10)$$

Where E_{ac} is an activation energy and $R_{c0} = R_{cry}$ when $T = T_{amb}$; both are model card parameters.

B. Model innovations

Equation (4) gives the time dependency of F_c , the parameter τ_c contains all other dependencies. In this study, the crystallization speed is considered dependent on the temperature and the amorphous fraction.

Considering (5), the crystallization speed $\partial F_c / \partial t$ can be extracted from (4) as a function of F_a and τ_c :

$$\frac{\partial F_c}{\partial t} = \frac{F_a}{\tau_c(T, F_a)} \quad (11)$$

To isolate the dependencies, we introduce v_g as the normalized amorphous-fraction-dependent growth speed and τ_{set} the temperature-dependent crystallization time:

$$\tau_c(T, F_a) = \tau_{set}(T) \cdot \frac{F_a}{v_g(F_a)} \quad (12)$$

1) Temperature dependent crystallization time

Ciocchini *et al.* [27] show that τ_{set} follows a non-Arrhenius behavior, because of an incompatibility of the activation energies between high and low temperatures. This is why in our approach, high- and low-temperature crystallization kinetics are separated, as given in equation (13):

$$\tau_{set} = \tau_{HT} + \tau_{LT} = \left(\tau_{0HT} e^{\frac{E_{AHT}}{kT}} + \tau_{0LT} e^{\frac{E_{ALT}}{kT}} \right) \quad (13)$$

Thereby, equation (13) enables the model to provide a good retention at room temperature and a short crystallization time during high-voltage pulses. Plotted in Fig. 3 is τ_{set} as a function of $1/kT$, with the temperature scale reported on the upper axis. This plot validates that the crystallization time is short at high temperature, whereas it is many orders of magnitude higher at room temperature.

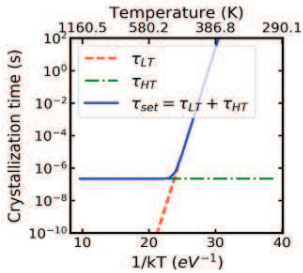


Fig. 3. Crystallization time as a function of temperature. τ_{set} is the sum of τ_{LT} and τ_{HT} , so that the process is quick at high temperature and slow at low temperature

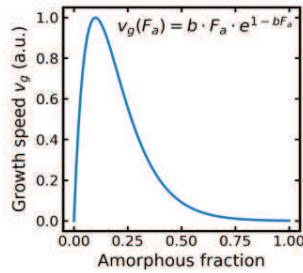


Fig. 4. Growth speed versus the amorphous fraction. This function is implemented to enhance the growth speed for low amorphous fraction.

2) Amorphous-fraction-dependent growth speed

The normalized growth speed v_g is inserted in the model to reflect the non-uniformity of the crystallization as a function of the size of the amorphous dome. As shown in Fig. 2, the simplified temperature calculated by the model is considered to

be the one at the interface between the heater and the GST. However, the temperature determining the crystallization process, considering re-growth from the surrounding crystalline GST ([19], [28]), is more likely the one at the external interface of the active volume. To take into account this effect while keeping a simple temperature calculation, we chose to let the growth speed vary with the amorphous fraction. Indeed, assuming a constant temperature gradient between the hot spot and the top electrode kept at room temperature, the temperature at the external interface moves with the position of this interface for a given input power. The smaller the amorphous dome, the closer the Amorphous/Crystalline interface is from the heater, and the warmer it is. The normalized growth speed v_g is defined by the expression shown in (14):

$$v_g(F_a) = b \cdot F_a \cdot e^{1-bF_a} \quad (14)$$

Where b is a fitting parameter. According to this expression, v_g at a given temperature is higher for low amorphous fractions, as shown in Fig. 4 where v_g versus F_a is plotted.

C. Electrical characterization method

The Transmission Electron Microscopy (TEM) cross-section, along with the equivalent scheme of the test structure is shown in Fig. 5. All characterizations are performed using this test structure. A wall-type PCM structure [29] is connected in series with a MOSFET selector, where the gate is used to limit the current flowing through the cell. u_a is the radius of the active volume, where phase transitions are located. This material switches from amorphous to crystalline and back to amorphous under the application of pulses. The whole device is integrated in a CMOS technology and the node between the PCM cell and the MOSFET selector is not accessible from outside. Therefore, the following results present the simulation of both devices in series, the MOSFET being previously extracted on a separately.

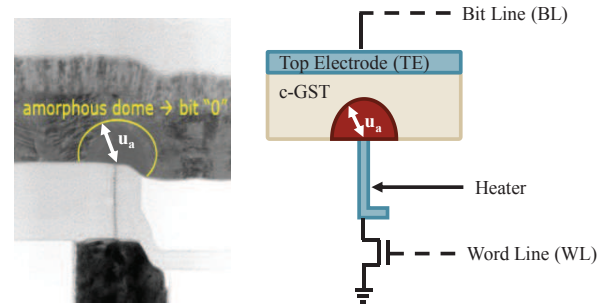


Fig. 5. TEM cross section of the test structure on the left hand side and equivalent schematics on the right hand side.

The characterization method aims to test every possible operating condition of the device in order to validate the model extensively. First, the current versus voltage is acquired for several intermediate states by setting the PCM into the desired state and applying a slow ramp voltage on the top electrode [23]. Then, the phase transitions are studied through three different characteristics, shown in Fig. 6; the RESET-SET-RESET is a staircase-up measurement with long squared pulses, the SET Low is a staircase-up with increasing pulse width in

the low current regime and the Rampdown SET is high current pulses with increasing fall times [30], [31].

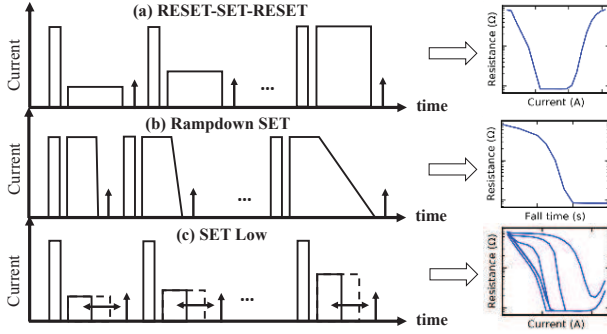


Fig. 6. Example of typical characteristics of PCM. Each point on the characteristics is composed of a RESET Pulse, a SET pulse and a DC reading: (a) RESET-SET-RESET is long squared pulses with increasing pulse current; (b) Rampdown SET is high current pulses with increasing fall times; (c) Set Low is a staircase-up with increasing pulse width in the low current regime.

Each measured point reported in these R-time or R-current characteristics is always composed of the same set of pulses, pictured in Fig. 7. First, a RESET operation is performed to fully control the initial state. Then a SET pulse, with a variable width, fall time and current amplitude, is applied to the cell and the programming current is measured. The programming current is averaged in the second half of the pulse width to avoid being disturbed by overshoots, when the current settles. As sketched in Fig. 7, the programming Word Line (WL) voltage is tuned in order to set the current value whereas the Bit Line (BL) voltage controls time width and fall time (FT) parameters. Finally the resistance value of the cell, which is a single point of measurement on the R-time or R-current characteristics, is extracted with 0.1V on the BL and 1.2V on the WL through a DC measurement.

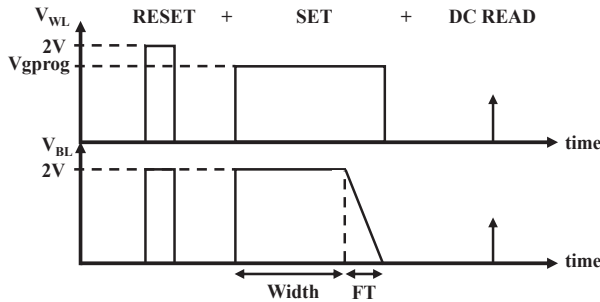


Fig. 7. Detail of the pulse sequence applied to get one measurement. WL programming voltage (V_{prog}), pulse width (Width) and fall time (FT) are the programming variables. Reading BL voltage is set at 0.1V. Delays between pulses are fixed to avoid drift effect issue

TABLE I
MEASUREMENT CONDITIONS

Variable	RESET-SET-RESET	Rampdown SET	SET Low
V_{WL}	0 – 2V	2V	0 – 1.2V
V_{BL}	2V	2V	2V
Current	0 – 300 μ A	300 μ A	0 – 200 μ A
Width	10 μ s	10 μ s	200n – 800ns
Fall time	10ns	10n – 600ns	10ns
Temperature	298 – 348K	298 – 348K	298 – 348K

These measurement conditions cover a wide range of the device operating and allow the full extraction of the model card parameters.

The measurement conditions used for each plotted characteristics are summarized in Table I. To get rid of the drift effect [32], the delay between the different pulses is constant. The impact of the ambient temperature is studied and error bars are obtained by repeating three times the exact same set of measurements.

III. MODEL VALIDATION THROUGH MODEL CARD EXTRACTION

The entire voltage range measured, including temperature and pulse time dependencies, is fitted using a single model card, which is shown in Table II. Given the simplifications made to ensure the fast convergence of the compact model, the model parameters do not correspond precisely to the physical parameters to which they are related. Yet, all model parameters have been kept to reasonable values during the extraction and they remain coherent with their associated physical parameters. They can be classified into three main categories: the first one is composed of the parameters related to the conductivity of the amorphous and crystalline phases, the second one includes the calculation of the temperature and the melting fraction inside the phase-change area, and the last category refers to time-dependent crystallization.

TABLE II
PHYSICAL AND FITTING PARAMETERS

Symbol	Description	Value
<i>Conduction parameters</i>		
A_{kPF}	Poole-Frenkel conduction prefactor	$6.5 \cdot 10^{-12} \Omega^{-1} \cdot m$
β_{PF}	Poole-Frenkel constant	$14 \mu eV \cdot V^{-0.5} \cdot m^{0.5}$
E_{a0}	Poole-Frenkel Activation Energy at 0K	0.2eV
u_{amax}	Maximum size of the amorphous dome	48nm
R_{c0}	Crystalline resistance at 0K	3k Ω
E_{ac}	Activation energy of the crystalline conduction	0.1eV
R_{heater}	Resistance of the heater	3.6k Ω
<i>Thermal parameters</i>		
C_{th}	Effective thermal capacitance	$10^{-16} J \cdot K^{-1}$
R_{thc}	Crystalline effective thermal resistance	$2.5 K \cdot \mu W^{-1}$
R_{tha}	Amorphous effective thermal resistance	$7.0 K \cdot \mu W^{-1}$
<i>Melting parameters</i>		
T_m	Melting temperature	960K
σ_m	Spread of the melting temperature	83K
τ_m	Characteristic melting time	1ns
<i>Crystallization parameters</i>		
τ_{0LT}	Crystallization time prefactor for low temperature	$2 \cdot 10^{-39} s$
E_{ALT}	Activation energy for low temperature	3eV
τ_{0HT}	Crystallization time prefactor for high temperature	220ns
E_{AHT}	Activation energy for high temperature	0.0eV
b	Fitting parameter	6

The whole characterizations have been modeled with this only set of parameters.

As the resistance is conditional upon the low field conduction, the I-V characteristics must be modeled first. The parameters A_{kPF} , u_{amax} and E_{a0} act respectively on the level, slope and temperature dependence of the amorphous subthreshold conduction. The threshold switching is modeled using a thermal runaway inside a Poole-Frenkel mechanism. Hence, tuning R_{tha} helps fitting the threshold switching. The SET resistance is modeled using R_{c0} and E_{ac} . The PCM current versus the Bit Line voltage for several intermediate states is shown in Fig. 8. No snapback is shown because the MOSFET voltage drop is not de-embedded. However, the MOSFET

model has been previously validated on a dedicated test structure, and the snapback capability of the model has already been demonstrated in our previous paper [23]. The model can simulate correctly the subthreshold conduction and the threshold switching for several intermediate states, with only one varying model parameter from one state to another, namely u_a . It validates the model for multilevel simulations.

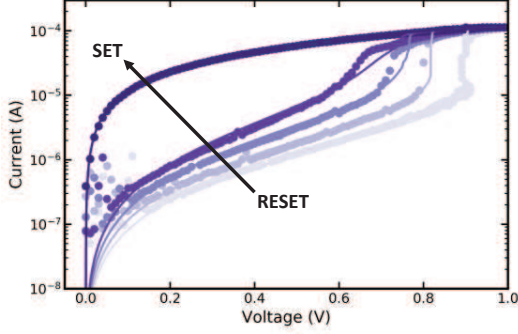


Fig. 8. Current of the PCM versus Bit Line voltage for several intermediate states, allowing the extraction of the conduction parameters. Dots are measurements, lines are simulations. The only parameter varying is the amorphous thickness u_a .

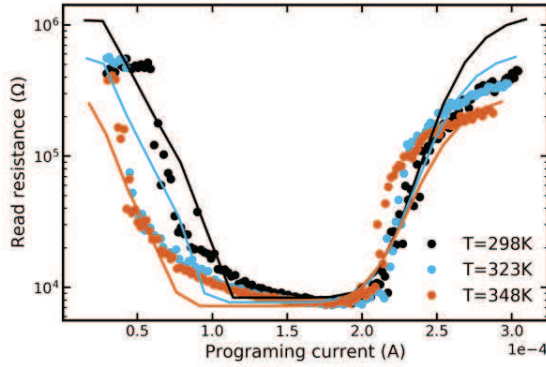


Fig. 9. RESET-SET-RESET characteristics: Staircase-up with long (10μs) pulses and sharp fall time (10ns) under three operating temperatures. Dots are measurements, lines are simulations. Both memory switching are visible on this characteristics and are correctly modeled.

The parameters belonging to the second category act on the RESET-SET-RESET characteristics, presented in Fig. 9. In this figure, the resistance is plotted as a function of the programming current for three different temperatures. The transitions RESET to SET and SET to RESET are well fitted considering the self-heating effect. We demonstrate that our model is able to reproduce the weak impact of external temperature as shown by experimental characterizations. All parameters dealing with both SET and RESET resistances have been previously extracted, using curves shown in Fig. 8. On the SET to RESET transition visible on the right hand side of these curves, the melting parameters T_m and σ_m are extracted. The time constant τ_m has not been measured, because it is shorter than the shortest measured pulse width, i.e. 200ns. It is set to 1ns, as previously described in the literature [25]. The RESET to SET transition is mostly determined by the parameters responsible for the crystallization at low temperature, namely τ_{OLT} and E_{ALT} . The parameter R_{thc} acts on the whole curve, since it is accountable for the temperature computation.

Once all static parameters are extracted, the dynamic behavior of the crystallization is studied on the Rampdown SET plot, presented in Fig. 10. The read resistance as function of the fall time is plotted for different programming currents on the left hand side, and for different temperatures on the right hand side. The transition for several temperatures and current levels is captured by the model using the parameters b , τ_{OHT} and E_{AHT} .

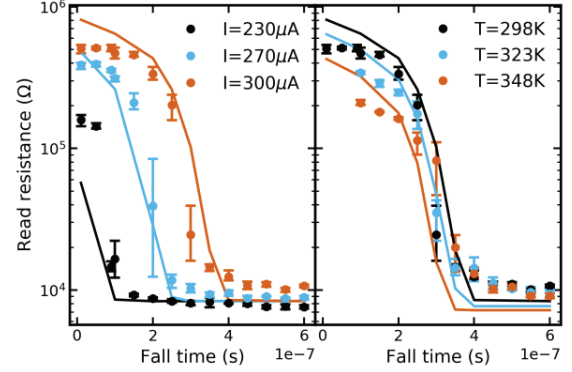


Fig. 10. Rampdown SET characteristics: Transition from RESET to SET using the fall time increase for three different programming current on the left, under three operating temperatures on the right. Dots are measurements, lines are simulations. Error bars are obtained by repeating three times the exact same set of measurements. The model reacts appropriately for both

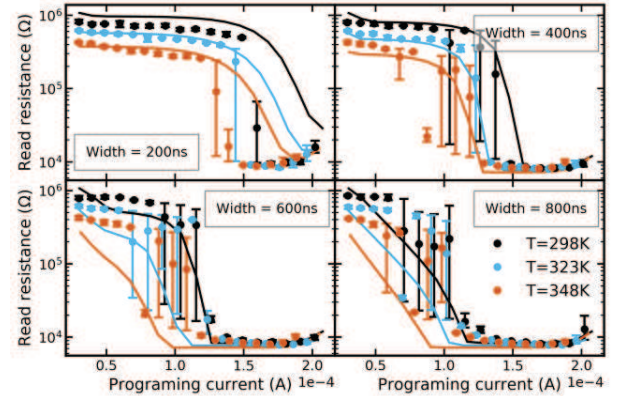


Fig. 11. SET Low characteristics: Transition from RESET to SET using low current density for four pulse widths under three operating temperatures. Dots are measurements, lines are simulations. Error bars are obtained by repeating three times the exact same set of measurements. The dynamics is hard to fit with the same model card as the Rampdown SET, as tradeoff has to be found to fit both characteristics.

The dynamics of the crystallization must also be checked on the SET Low characteristics, where the SET operation is realized at relatively low current but depends on the pulse width. The SET Low results are shown in Fig. 11, exhibiting the phase transition for pulse widths ranging from 200ns to 800ns for three different ambient temperatures. The ambient temperature variation has an important impact on the high resistive conduction, in both the model and the measurements, and it seems that crystallization happens earlier at high ambient temperature in both the measurements and in the model. However, error bars in the transition regime means that the transition happens abruptly and stochastically in the transition regime. The modeling of this transition is smooth, because the model is built on state variables that always vary continuously. This stochasticity, which has been reported by Le Gallo *et al.* [33], will be integrated in future development using corners.

The modeling of the SET Low characteristics is done using the same crystallization parameters as the Rampdown SET, *i.e.* b and τ_{OHT} . Hence, a tradeoff has to be found between those two fits. The thermal activation E_{AHT} can be optimized, as well as the ratio R_{tha}/R_{thc} , so that all features are well fitted.

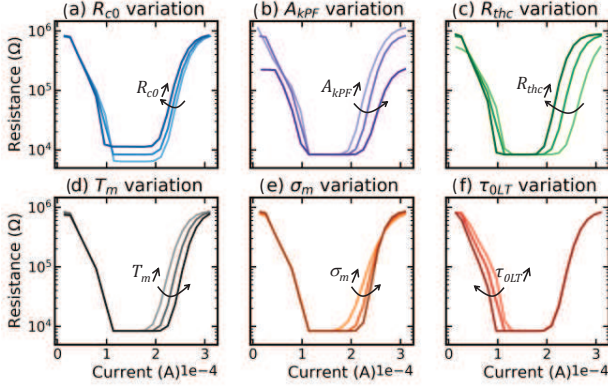


Fig. 12. Impact of the static parameters on the RESET-SET-RESET characteristics. (a) R_{c0} rules the conduction in the SET regime; (b) A_{kpf} impacts the RESET resistance; (c) R_{thc} increases the internal temperature, which is mostly seeable in the melting phase; (d) The average melting temperature T_m impacts the SET to RESET transition current; (e) σ_m changes SET to RESET transition spread; (f) τ_{0LT} deals with RESET to SET transition.

IV. PARAMETER PHYSICAL MEANING

After the model is validated, the variation of the model card parameters is shown in order to illustrate their impact and physical meanings. Let us consider the RESET-SET-RESET characteristics, as pictured in Fig. 12. The level of the crystalline resistance is dependent on A_{kpf} , the Poole-Frenkel pre-factor. R_{thc} plays on every aspect of this curve, as it rules the internal temperature. The SET to RESET transition proceeds of the amorphisation of the material, which involves the melting of it first. As the fall time is short in this experiment, the crystal does not have time to grow and the material stays in the disordered phase. The level of resistance achieved only depends on the amount of material that has been melted during the pulse. A change in the melting temperature T_m shifts the transition whereas a modification of the σ_m parameter modifies the slope of the transition. Finally, the parameter τ_{0LT} dominates the RESET-SET transition because the operation happens in the model at a quite low temperature.

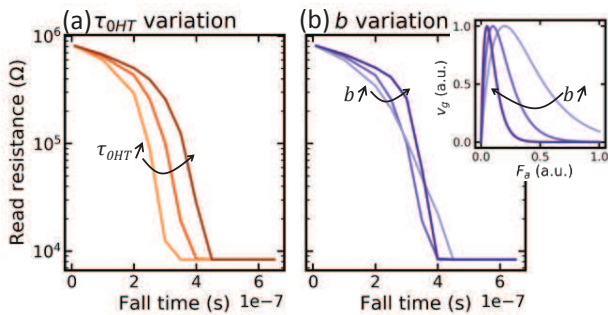


Fig. 13. Impact of the variation of the parameters τ_{OHT} and b on the growth speed. (a) τ_{OHT} acts on the mean crystallization time; (b) b increases the growth speed for low amorphous fraction (inset), so enhances the positive feedback on the Rampdown SET crystallization speed.

Fig. 13 highlights the details of the Rampdown SET operation through the variation of two effective parameters τ_{OHT} and b . τ_{OHT} impacts the average crystallization time, as illustrated in Fig. 13(a). As displayed in the inset of Fig. 13(b), b accentuates the growth speed for low amorphous fraction, thus accelerates the crystallization process as the crystallization fraction increases. This auto-positive feedback sets the abruptness of the transition that can be seen in Fig. 13(b).

Both Rampdown SET and SET Low operations are modeled by the same mechanism, which is the growth from the surrounding crystalline GST. In order to satisfy both crystallization dynamics with the same set of parameters, two levers are used. First, the temperature activation of the crystallization time can be tuned because both crystallizations do not happen at the same internal temperature. Second, we can use the concurrency between both thermal resistances, R_{tha} and R_{thc} . Inspired by finite element simulations done by Cueto *et al.* [19], the lever consists of enhancing the crystallization speed at low current by artificially increasing the internal temperature immediately after the threshold switching using a strong R_{tha} . On the contrary, a lower R_{thc} will slow the crystallization at high current, as the temperature achieved in the cell will be lower.

V. PERFORMANCE ASSESSMENT

The performance of the model, measured in simulation time, is now discussed. To check this aspect, addressable matrixes of PCM, including the MOSFET selector, have been simulated using the Mentor Graphics' simulator Eldo on a single 2.60GHz Intel® Xeon® CPU E5-2697 v3. Simulating 10 bits takes half a second and the multiple thread processing of a 10 Kbits matrix on 4 CPU can take just about 12 minutes, for a full RESET/SET/READ sequence. This simple example proves that this model is completely suitable for circuit simulation, because it is accurate and allows fast simulation, even for multiple cells.

VI. CONCLUSION

A new comprehensive compact model is proposed. It is compared to extensive measurements covering a wide range of times, currents, and operating temperatures. Our model fits well to all the electrical characterization results using a single model card, including for the first time a compact modeling of two different crystallization dynamics, named Rampdown SET and SET Low. This is possible using several modeling innovations that have never been used before, such as the explicit use of a melting fraction, a non-Arrhenius form of the crystallization time and a growth speed enhanced for low amorphous fractions. The physical effects described in this model help to model the different crystallization dynamics independently on the temperature and programming current variations. A switchless Verilog-A implementation of the physical-based equations ensures the fast convergence of the model, even out of the fitting range. Tests run on multiple addressable matrixes exhibit reasonable simulation times, proving that the model is suitable for circuit simulation, thanks to the efficient implementation which enables short convergence time.

VII. REFERENCES

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